REMARKS

The Applicant respectfully requests further examination and reconsideration in view of the amendments made above and the comments set forth below. Within the Office Action, claims 1-10 and 18-28 have been rejected. By the above amendment, claims 1, 5, 9, 18, 21-23, and 26-28 have been amended and claims 2, 3, 7, 8, 19, and 20 have been canceled. Accordingly, claims 1, 4-6, 9, 10, 18 and 21-28 are pending.

Rejections under 35 U.S.C. § 103(a)

Within the Office Action, claims 1-10 and 18-28 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent Number 5,605,853 to Yoo *et al.* (hereinafter "Yoo") in view of U.S. Patent Number 5,679,559 to Mehta (hereinafter "Mehta"). The Applicant respectfully disagrees with this rejection.

Yoo teaches a method of forming an SRAM, a floating gate memory, and a logic device on the same integrated circuit. Specifically, Yoo teaches a method of forming simultaneously an SRAM and an EEPROM on the same integrated circuit, using a LOCOS isolation process. [Yoo, col 3, lines 51-55]. Yoo teaches a method of forming a plurality of field isolation regions using a LOCOS isolation process. [Yoo, col 3, line 55-60] The structure disclosed in Figure 7 of Yoo comprises an SRAM 50 and a gate memory 70 separated by field oxidation regions 12.

Yoo does not teach or suggest that a SRAM and an EPROM can be formed on the same IC, using a shallow trench isolation (STI) process. Neither does Yoo teach or suggest that an SRAM and an EPROM can be formed on the same IC, using a combination of a LOCOS and an STI isolation process. As indicated by Yoo, in column 2, lines 18-26, a combination of an SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* [Yoo, column 2, lines 23-26] In column 2, lines 18-26, Yoo states:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining an SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Further, Yoo teaches away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate.

Mehta teaches a device and method for isolating regions of a circuit device in a semiconductor substrate. The method comprises the following steps: forming a first insulation region and a second insulation region; etching a trench in the first insulation region, the trench extending into the semiconductor substrate to a depth below the surface of the substrate; filling the first isolation region with an isolation material and removing a portion of the isolation material such that the trench isolation material fills the trench and has a surface level with the surface of the substrate; and thermally growing a field oxide in the first and second isolation regions. [Mehta, Abstract and col. 4, line 46 to col. 6, line 49]

Mehta does not teach or suggest combining a LOCOS isolation structure and an STI isolation structure. Instead, Mehta teaches a LOCOS region and a field oxidized trench region. (*see, e.g.*, Mehta, col. 6, lines 21-22), not an STI region. At column 7, lines 42-25, Mehta makes clear that it does not teach STI: "Finally, in shallow trench isolation, a critical planarization mask is generally needed to reduce such dishing. *In the present method and apparatus*, no such critical mask is needed" (italics added).

Indeed, Mehta teaches against using STI structures in general. For example, at column 2, lines 50-58, Mehta states:

> However, shallow trench isolation (STI) is relatively complex because an anisotropic etch must be used to define the trench, the trench must be etched deeply into the silicon, and filling the trench with the isolation material can raise additional processing issues in preparing the integrated circuit. STI also results in relatively sharp corners at the edges of the trench at the silicon surface. This can result in electrical field leakage at these corners and gate oxide quality problems.

In the Summary of the Invention, Mehta states that one "object of the invention is to provide a process which provides significant advantages over shallow trench isolation and combination of shallow trench isolation and local oxidation processes." [Mehta, col. 3, lines 56-59] Later, Mehta states that "[STI] technology . . is replete with problems." [*Id.*, col. 7, lines 21-22]

Mehta distinguishes its invention over STI, and thus teaches way from STI, by stating that its invention "preserves the familiar and well-characterized interface between active regions and isolation regions in the LOCOS field. No edge oxide quality problems would therefore result." [*Id.*, lines 26-29] Mehta further states that "[STI] is subject to trench corner leakage" (*id.*, line 30-31) and produces "dishing [which causes] thinning of the isolation in wide-trench regions" (*id.*, lines 38-39). Thus, Mehta teaches away from structures that use STI structures alone or in combination with any other isolation structures.

Within the Office Action, it is concluded that it would have been obvious to use the STI isolation technique as taught by Mehta in the substrate of Yoo. The applicant respectfully disagrees with this conclusion. As discussed above, Mehta teaches away from the use of STI. Further, to support this conclusion, a *prima facie* case of obviousness must be demonstrated. No such demonstration has been made here. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation demonstrated, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the teachings of the references. Second, there must be a demonstration that the combination of the prior art references would result in a reasonable expectation of success. Third, the combination of the prior art references must teach or suggest all the claim limitations. [M.P.E.P § 2142 - 43.]

First, there is no suggestion or motivation to combine Yoo and Mehta. Yoo teaches away from including a SRAM and an EPROM on the same IC, isolated by a combination of a LOCOS and a second isolation technique. Furthermore, Mehta does not teach or otherwise indicate that the first and second isolation techniques can be applied to isolate a SRAM and an EEPROM on a common IC. Therefore, it would not have been obvious to one skilled in the art to combine the teachings of Yoo and Mehta. The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Within the Office Action, there has not been any reference to any teaching, hint or suggestion in either Yoo or Mehta suggesting the desirability of combining these two references.

Further, there is no indication in the prior art that a combination of Yoo and Mehta would result in a reasonable expectation of success. As indicated by Yoo, in column 2, lines 18-26, a combination of a SRAM and EEPROM on the same IC is desirable. *However, Yoo specifically teaches that such an IC is difficult to fabricate because of the difference in fabrication processes.* [Yoo, column 2, lines 23-26] Furthermore, the teachings of Mehta do not indicate or suggest that the first and second isolation techniques can be applied to isolate a SRAM and an EPROM on a common IC. The combination of the teachings of Yoo and Mehta would not have resulted in a reasonable expectation of success. Therefore, the combination of the teachings of Yoo and Mehta does not render the current invention obvious.

Even if considered proper, the combination of Yoo and Mehta does not teach the claimed invention. In contrast to the teachings of Mehta, Yoo and their combination, the present invention teaches a system for *independently* or *non-concurrently* integrating SRAM cells and flash EPROM cells onto a single silicon substrate. As discussed above, neither Mehta, Yoo nor their combination teaches or suggests forming a SRAM and an EPROM on a single substrate using a combination of a LOCOS and STI isolation process. In column 2, lines 18-26, Yoo states the following:

> It may be also desirable to form more than one type of memory structure on the same IC, such as an SRAM in conjunction with an EEPROM (Electrically Erasable Programmable Read Only Memory), as well as logic devices. However, such an IC is difficult to fabricate due to the difference in the typical processes for forming memory and logic and for forming significantly different memory devices.

This statement suggests that Yoo's invention is directed to a method of combining a SRAM and an EEPROM on the same IC, when the same LOCOS isolation process is used on all the regions of the substrate. By this statement, Yoo further concedes that his method does not solve the difficulty of fabricating an SRAM and an EPROM on the same substrate. Rather, Yoo suggests that an alternative to finding a method of combining two methods would be to improve the current LOCOS isolation method so as to be used on both the SRAM and EEPROM. Therefore, it would not have been obvious to one skilled in the art, that Yoo could have been combined with Mehta to disclose the current invention. Further, Yoo appears to be teaching away from using multiple different isolation processes on a single IC. Yoo acknowledges the inherent difficulty of applying multiple different isolation processes on an IC, and does not suggest or teach applying a LOCOS and STI isolation process on the same substrate. Therefore it would not have been obvious to one skilled in the art from the teachings of Yoo, that a LOCOS and STI isolation process could have been used to form a SRAM and an EEPROM on a common

substrate. Further, as discussed above, Mehta teaches away from the use of the STI isolation technique.

The present invention is directed to semiconductor devices and systems comprising an SRAM device and an EPROM device on a single substrate. The SRAM device is formed on an STI isolation structure and the EPROM device is formed on a LOCOS isolation structure. The present invention thus provides on a single substrate both low-voltage devices and high-voltage devices. Such a structure has the advantages of smaller package size, less interference, and quicker transmission of data between the SRAM and EPROM cells. [Specification, page 10, line 24, to page 11, line 4]

The independent claim 1 is directed to a semiconductor device. The semiconductor device of claim 1 comprises a common substrate, an SRAM device implemented on the common substrate and isolated by an STI isolation structure, and a flash EPROM device implemented on the common substrate and isolated by a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently. As discussed above, neither Yoo, Mehta nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. Within the Office Action it is stated that "Mehta discloses the first [isolation] technique is the STI technique and the second isolation technique is LOCOS isolation, as discussed in claim 1." The Applicant respectfully disagrees with this statement. Instead, Mehta teaches a LOCOS region and a field oxidized trench region. As discussed above, Mehta teaches away from using an STI isolation structure. For at least these reasons, claim 1 is allowable over the teachings of Yoo, Mehta and their combination.

Claims 2 and 3 have been canceled by the above amendment. Claim 4 is dependent on the independent claim 1. As discussed above, claim 1 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 4 is also allowable as being dependent on an allowable base claim.

The independent claim 5 is directed to a system containing different types of isolation structures. The system of claim 5 comprises a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently, an SRAM device on the first portion of the substrate, and a flash EPROM device on the second portion of the substrate. As discussed above, neither Yoo, Mehta nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI

isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. For at least these reasons, claim 5 is allowable over the teachings of Yoo, Mehta and their combination.

Claims 7 and 8 have been canceled by the above amendment. Claim 6 is dependent on the independent claim 5. As discussed above, claim 5 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 6 is also allowable as being dependent on an allowable case claim.

The independent claim 9 is directed to a semiconductor device. The semiconductor device of claim 9 comprises a common substrate having a first portion including an STI isolation structure and a second portion including a LOCOS isolation structure, wherein the STI isolation structure and the LOCOS isolation structure are implemented non-concurrently, an SRAM device implemented on the first portion of the substrate, and a flash EPROM device implemented on the second portion of the substrate. As discussed above, neither Yoo, Mehta nor their combination teaches or suggests a common substrate having a first portion with an STI isolation structure and a second portion with a LOCOS isolation structure. For at least these reasons, claim 9 is allowable over the teachings of Yoo, Mehta and their combination.

Claim 10 is dependent on the independent claim 9. As discussed above, claim 9 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claim 10 is also allowable as being dependent on an allowable case claim.

The independent claim 18 is directed to a semiconductor device. The semiconductor device of claim 18 comprises a common substrate, a first portion formed on the common substrate, and a second portion formed on the common substrate. The first portion comprises an SRAM device over a first single device layer, the first single device layer comprising a first active region and an STI isolation structure. The second portion comprises a flash EPROM device over a second single device layer, the second single device layer comprising a second active region and a LOCOS isolation structure. As discussed above, neither Yoo, Mehta nor their combination teaches or suggests a structure on a single substrate having an EPROM device over a first single device layer that contains an active region for the EPROM device and a LOCOS isolation structure and an SRAM device over a second single device layer that comprises an active region for the SRAM device. As discussed above, neither Yoo, Mehta nor their combination discloses a single substrate having an EPROM device isolated using a LOCOS isolation structure and an SRAM device isolated using an STI isolation structure. Further, neither Yoo, Mehta nor their combination discloses a structure with a single device layer having both an active region and an isolation structure. Figure 18 of Mehta discloses a structure with one device layer (e.g., 110) containing the active region and a second device layer (e.g., 240)

containing the isolation structure. Figure 5 in Yoo discloses a structure with one device layer for the isolation structure (e.g., field oxide region 12) and another device layer (e.g., substrate 10) containing the active region 22. For at least these reasons, claim 18 is allowable over the teachings of Yoo, Mehta and their combination.

Claims 19 and 20 have been canceled by the above amendment. Claims 21 and 22 are dependent on the independent claim 18. As discussed above, the independent claim 18 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claims 21 and 22 are both also allowable as being dependent on an allowable base claim.

The independent claim 23 is directed to a semiconductor device. The semiconductor device of claim 23 comprises a common substrate, an SRAM device implemented on the common substrate and formed over a first active region on a first isolated structure including an STI isolation structure, and a flash EPROM device implemented on the common substrate and formed over a second active region on a second isolated structure including a LOCOS isolation structure. It is further specified in claim 23 that the second isolated structure has an outer portion extending a first depth into the substrate and an inner portion containing the second active region and extending a second depth into the substrate, the first depth larger than the second depth. As discussed above, neither Yoo, Mehta nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion containing an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. Instead, Mehta discloses a structure in which a structure contains an inner portion extending a first depth into a substrate and an outer portion extending a second depth into the substrate, where the second depth is larger than the first depth, thus resulting in a bird's beak. Yoo discloses a similar structure. Further, as discussed above, neither Yoo, Mehta nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. For at least these reasons, claim 23 is allowable over the teachings of both Yoo, Mehta and their combination.

Claims 24 and 25 are both dependent on the independent claim 23. As discussed above, the independent claim 23 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claims 24 and 25 are both also allowable as being dependent on an allowable base claim.

Claim 25 is further directed to a structure having the first isolated structure contiguous with the second isolated structure. Such a structure leads to an even smaller device package. Neither Yoo, Mehta nor their combination teaches or suggests such a structure. Figure 18 in

Mehta discloses a first structure 242 and a second structure 240 separated by a region 110. The two structures are not contiguous. Similarly, Yoo discloses field oxide regions 12 separated by the substrate 10 and doped layers 22. The regions 12 are not contiguous. For this additional reason, claim 25 is allowable over the teachings of Yoo, Mehta and their combination.

The independent claim 26 is directed to a system containing a semiconductor device having a plurality of isolated structures. The system of claim 26 comprises a common substrate having a first area including an STI isolation structure and a second area including a LOCOS isolation structure, the second area having an outer portion extending a first depth into the substrate and an inner portion including an active region extending a second depth into the substrate, wherein the first depth is larger than the second depth, an SRAM device implemented on the first area of the substrate and a flash EPROM device implemented on the second area of the substrate. As discussed above, neither Yoo, Mehta nor their combination teaches or suggests an isolated structure having an outer portion extending a first depth into a substrate and an inner portion containing an active region and extending a second depth into the substrate, where the first depth is larger than the second depth. Instead, Mehta discloses a structure having an inner portion extending a first depth into a substrate and an outer portion extending a second depth into the substrate, where the second depth is larger than the first depth, thus resulting in a bird's beak. Yoo discloses a similar structure. Further, as discussed above, neither Yoo, Mehta nor their combination teaches or suggests a common substrate having an SRAM device isolated by an STI isolation structure and a flash EPROM device isolated by a LOCOS isolation structure. For at least these reasons, claim 26 is allowable over the teachings of Yoo, Mehta and their combination.

Claims 27 and 28 are both dependent on the independent claim 26. As discussed above, the independent claim 26 is allowable over the teachings of Yoo, Mehta and their combination. Accordingly, claims 27 and 28 are both also allowable as being dependent on an allowable base claim.

Claim 27 is further directed to a system having the first isolated structure contiguous with the second isolated structure. Such a structure leads to an even smaller device package. Neither Yoo, Mehta nor their combination teaches or suggests such a structure. Figure 18 in Mehta discloses a first structure 242 and a second structure 240 separated by a region 110. The two structures are not contiguous. Similarly, Yoo discloses a field oxide regions 12 separated by the substrate 10 and doped layers 22. The regions 12 are not contiguous. For this additional reason, claim 27 is allowable over the teachings of Yoo, Mehta and their combination.

For the reasons given above, the Applicant respectfully submits that the claims are in a condition for allowance, and allowance at an early date would be appreciated. If the Examiner has any questions or comments, the Examiner is encouraged to call the undersigned at (408) 530-9700 to discuss them so that any outstanding issues can be expeditiously resolved.

Respectfully submitted,
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